PLASMA in INDUSTRY

MICROELECTRONICS (etching, PE-CVD, etc)

SiOx ctngs in many applications

STERILIZATION in hospital

...

PLASMA SOURCES in Plasma Medicine

INDUSTRIAL AREAS of COLD PLASMAS

> MICROELECTRONICS SEMICONDUCTORS SOLAR CELLS LIGHT SOURCES OZONE PRODUCTION AUTOMOBILE FOOD PACKAGING TEXTILE BIOMATERIALS MICROFLUIDICS MEMS CLEANING STERILIZATION BIOLOGY ENVIRONMENT

CATALYSIS MEDICINE POLYMERS PAPER WETTABILITY ADHESION METALLIZATION PRINTING, DYEING CORROSION PROTECTION CULTURAL HERITAGE COMPOSITES SENSORS OPTICS BUILDINGS



MICROELECTRONICS etching, PE-CVD, etc















Solar grade silicon cannot be used for microelectronics.

To properly control the quantum mechanical properties of silicon, bulk Si wafers used in the IC making process must first be refined to 99.9999999 % ("9N", "9 nines"), which requires repeated refining.

Most Si crystals for device production are produced with the **Czochralski process**, (Cz-Si). Single crystals grown in this way contain impurities dissolved from the crucible, and need to be refined with the **melting zone technique**.



SC and IC industry use wafers with standard dimensions, a few inches wide in early days, **200 and 300 mm dia** today. The width is controlled by precise control of temperature, rotation speeds and withdrawn rate of the seed holder. The crystal ingots from which wafers are sliced can be 2 m long, hundreds Kg heavy.

Si wafers, introduced in the 1940's, are 0.2 – 0.75 mm thick, polished to great flatness for IC, or textured for solar cells. Larger wafers improve the manufacturing efficiency, with more chips fabricated per wafer. Wafers up to 450 mm dia are used.

When Si is fully melted, at about 1500°C, a small seed crystal mounted at the end of a rotating shaft is slowly lowered until it just dips below the surface of molten Si. The atmosphere of the chamber has to be inert. The shaft rotates counterclockwise and the crucible clockwise. The rotating rod is then drawn upwards very slowly, forming a rough cylinder, 1-2 m long, depending on the amount of Si in the crucible.

The electrical characteristics of Si are controlled by adding **P** or **B** dopants, a method also used with GaAs and other SCs. Si ingots are refined and purified to the electronic grade with the melting zone technique.







Si crystal grown by Czochralski process at Raytheon, 1956. The induction heating coil is visible, and the end of the crystal just emerging from the melt. The technician is measuring the temperature with an optical pyrometer. In the earliest Si plants, crystals produced by this early apparatus were only one inch wide.



At the solid/liquid boundary, the impurity atoms will diffuse to the liquid zone. Thus, by passing a crystal rod through a thin section of furnace very slowly, only a small region is molten at any time, and impurities segregate at the end of the rod. The rod can grow as a perfect single crystal if a seed crystal is placed at the base to initiate a chosen direction of crystal growth. When high purity is required, the impure end of the rod is cut, and the refining is repeated.

V. M. Donnelly, A. Kornblit Plasma etching: yesterday, today, and tomorrow J. Vac. Sci. Technol. A, Vol. 31(5), 2013

Plasmas have been used to etch fine features in Si Integrated circuits for 50 years. Without this technology, we would be stuck in the 1970s, listening through tinny headphones to disco music on our "small" portable cassette tape player. Carrying laptops around would be more for fitness than for convenience, and mobile "smart" phones would require wheels. Today we take these marvels for granted.

The first commercially available microprocessor, the **Intel 4004**, a 4 bit processor, was launched in 1971 with 2300 transistors, operated at 1.08 MHz clock frequency, with minimum feature size of **10** μ m. Intel 3rd generation multicore processors, launched in 2012, are 64 bit processors, contain 1.4x10⁹ transistors, operate at about 3 GHz clock-frequency, and use **22 nm** minimum feature size.

A key element contributing to advances in microprocessors was the ability to fabricate smaller transistors, due to advancements in lithography and pattern-transfer methods.

In the early days of IC fabrication, pattern-transfer was accomplished by wet etching. However, with time, **plasma etching became the preferred pattern-transfer method**.





Moore's Law – The number of transistors on integrated circuit chips (1971-2018)



Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore's law.







1993 vs 2013

教出部的和法院结婚的正言



Nobel prize for Physics year 2000



Nobel Prize recognizes pioneers of the modern semiconductor industry

Fundamental building blocks of the modern semiconductor industry have been recognized in this year's Nobel Prize for Physics. The annual prize was awarded jointly to Jack Kilby of Texas Instruments for his invention of the integrated circuit, and to Zhores Alferoy and Herbert Kroemer for developing semiconductor heterostructures used in high-speed electronic devices and optoelectronics. Alferov is director of the AF loffe Physico-Technical Institute in St Petersburg, Russia, while Kroemer is professor of physics at the University of California in Santa Barbara.

The Royal Swedish Academy of Sciences – which awards the prize to scientists who have "made the most important discovery or invention within the field of physics" has recognized the basic work by



In the beginning - the first integrated circuit that Jack Kilby built

these scientists in information and communications technologies. The prize is worth SEK 9 million: Kilby will receive half, while Alferov and Kroemer will share the rest.

Kilby is recognized for his part in inventing the integrated circuit. He showed in 1958 that a complete circuit could be fabricated in a single piece of germanium. Meanwhile, Robert Noyce at Fairchild Electronics – later to became Intel – developed a method to create an integrated circuit in silicon using aluminium as conducting strips.

Alferov and Kroemer are honoured for inventing high-speed transistors and optoelectronic components based on multilayered structures of compound semiconductors. These devices have allowed the development of semiconductor lasers and lightemitting diodes, and also underpin the explosive growth in the communications sector.

 The Nobel Prize for Chemistry recognizes more recent developments in the semiconductor industry. It was awarded to Alan Heeger of the University of California in Santa Barbara, Alan MacDiarmid of the University of Pennsylvania and Hideki Shirakawa of the University of Tsukuba in Japan for discovering that plastic materials can be made to conduct electricity efficiently. Their discovery is fuelling the current drive to produce plastic versions of electronic devices such as light-emitting diodes and displays.



After Isotropic Etch

WET ETCHING

Advantages:

- Simple equipment
- High throughput (batch process)
- High selectivity

Disadvantages:

- Isotropic etching leads to undercutting
- Uses relatively large quantities of etch chemicals, must immerse wafer boats, must discard partially used etch to maintain etch rate
- Hot chemicals create photoresist adhesion problems
- Small geometries difficult, line with > thickness, etch block caused by surface tension
- Critical Etch time, dimensions change with etch time, bias develops
- Chemical costs are high
- Disposal costs are high

- Silicon (Nitric Acid and Hydrofluoric Acid and water)
 - Si +HNO3 + H2O --> SiO2 + HNO2 +H2 (+6HF) --> H2SiF6 + HNO2 + 2H2O + H2
- SiO2 (HF Water and NH4F)
 - SiO2 + 6HF --> H2 +SiF6 +2H2O
- Si3N4 (Dilute Hot Phosphoric (180C) H3PO4)
- Al (HPO4) +HNO2 +Acedic CH3COOH + H2O
 - Nitric oxidizes Al --> Al2O3 and HPO4 dissolves Al2O3



dry etching has completely taken the place of wet etching

a layer can not be etched if it does not form volatile products

PLASMA "DRY" ETCHING

reaction between a solid and a gas reactant (the "etchant") with formation of volatile products



- a) Directional Etching anisotropic
- b) Isotropic Etching

FIG. 2. Schematic of (a) directional etching, showing a greater rate of material removal in the vertical direction than lateral, and (b) isotropic etching, showing material removed at the same rate in all directions.



FIG. 1. Schematic diagram of the apparatus used to study ion-assisted gassurface chemistry. The gas injection tube is 1.6 mm inside diameter and is about 3 mm from the quartz crystal microbalance. The gas flow is determined from the rate of pressure increase in the reservoir when the shut-off valve is closed.

J.W. Coburn, H.F. Winters, J. Vac. Sci. Tech. 16, 391, 1979





Si (fragments) \uparrow slow (sputtering) C) Si \rightarrow





Figure 1.2 Positive and negative resist: exposure, development, and pattern transfer. Positive resists develop in the exposed region. Negative resists remain in the exposed region.

Microelectronics: from sand to chips





Figure 5.26 SEM micrograph of HEXSIL tweezers: 4 mm long, 2 mm wide, and 80 μ m tall. Lead wires for current supply are made from Ni-filled poly-Si beams; *in situ* phosphorus-doped polysilicon provides the resistor part for actuation. The width of the beam is 8 μ m: 2 μ m poly-Si, 4 μ m Ni, and 2 μ m poly-Si. (Courtesy of Dr. C. Keller, MEMS Precision Instruments.)





Directionality of Etching



Anisotropic Etch (x < z) 0 < A < 1





Vertical Etch (x = 0) A = 1 (Perfectly anisotropic)

isotropic with mask erosion

Why Plasma Etching?

Advanced IC Fabrication with small geometries requires precise pattern transfer

Geometry in the < 1.0 micrometer range is common

Line widths comparable to film thickness

Some applications require high aspect ratio

Some materials wet etch with difficulty

Disposal of wastes is less costly

Dry Etching Characteristics

Advantages:

- No photoresist adhesion problems
- Anisotropic etch profile is possible
- Chemical consumption is small
- Disposal of reaction products less costly
- Suitable for automation, single wafer, cassette to cassette

Disadvantages:

- Complex equipment, RF, gas metering, vacuum, instrumentation
- Selectivity can be poor
- Residues left on wafer, polymers, heavy metals
- Particulate formation
- CFC's

DRY ETCHING GENERAL MECHANISM

- Generation of etchants in the plasma
- Diffusion of etchants to the substrate surface
- Adsorption (and migration) of etchants
- Reaction between substrate and etchant
- Desorption of by-products
- Diffusion of by-products to the gas phase

each step is characterized by a ΔH and can be influenced by the ion bombardment



Etching Gas & By-Products

Solid	Etch Gas	Etch Products
Si, SiO2, Si3N4	CF4, SF6, NF3	SiF4, Si2F6,
Si	CI2, CCI2F2	SiCl4, SiCl2,
AI	BCI3, CCI4,	AI2CI6, AICI3
Refractory Metals (W, Ta, Nb, Mo)	CF4, CI2	WF6, WCI6
Organic Solids	02, 02+CF4	CO, CO2, HF, H2O,
III-V (GaAs, InP)	CI2, CCI2F2	Ga2Cl6, GaCl3, AsCl3
II-VI (HgCdTe, ZnS,)	CH4 + H2	Zn(CH3)2, H2S

sputtering

chemical





ion assisted **Pi.a. < Ps.i.** sidewall inhibitor



Low Density Plasma Reactors

Plasma Etcher

- Plasma Etching Mode in Parallel Plate or Planar Reactor
- Wafer placed on the Grounded Electrode
- Capacitively Coupled Plasma



- Isotropic by Radical
- Plasma Potential (Low Ion Energy)
- High Pressure
 - Single Wafer Type
 - Less Electrical Damage
 - Reinberg Reactor

Medium Density Plasma Reactors

RIE Etcher

- Reactive Ion Etching (RIE) = Plasma Etching + Energetic Ion Bombardment
- Reactive Ion Etching (RIE) = Reactive Sputter Etching (RSE)
- Wafer placed on the RF-driven Electrode
- Capacitively Coupled Plasma



- Anisotropic by Ion
- DC Self-bias
 - (High Ion Energy)
- Middle Pressure
- Single Wafer Type
- Electrical Damage

Medium Density Plasma Reactors

MERIE Etcher

- Magnetic field is above and Parallel to the cathode surface
- Keep the Secondary Electron by Cycloidal Motion in ExB Field
- Probability for electron-neutral collisions can be increased
- Ionization efficiency in Dark Sheath Region is increased



- B field is rotated electrically
 Anisotropic by Ion
- Low Pressure
 - Single Wafer Type
 - Lower Electrical Damage

High Density Plasma Reactors

Ex)TCP : Lam Research



<Characteristics>

- Low Pressure Control ≤ 5mT
- Independent Power Control
 - Plasma Source = TCP power
- High Density Plasma $\sim 10^{\,12}$
- Ion DC Bias = Bias Power
- Low Temperature Etching
 - : -50°C \sim +50°C
- Improved Plasma Uniformity

High Density Plasma Reactors

ECR (Electron Cyclotron Resonance)

Cyclotron Resonance = Maximum Electron Energy Angular Frequency in B field (875G) = Microwave Frequency (2.45GHz)



bias potential







distance



Effect of the bias-induced positive-ion bombardment on the deposition / etching rate of CFx films plasma-deposited in RF glow discharges ($CF_4 0.8 / C_2F_4 0.2$ feed).

Α

Adapted from F. Fracassi, J.W. Coburn, J. Appl. Phys. 63, 1758, 1988.

FACTORS AFFECTING DRY ETCHING

1. Neutrals (active species)

gas feed, flow rate power (fragmentation) pressure

- 2. Substrate temperature
- 3. Substrate position
- 4. lons (positive)

5. Surface contamination

substrate bias reactor geometry power pressure

{ polymer, resist residues
 inorganics
 non volatile etch products

SUBSTRATE POSITION IN THE REACTOR IS IMPORTANT



EFFECT OF T and CONCENTRATION

E_R depends on the rate limiting step

 $E_R = A N_X e^{-Ea/RT}$

 N_x = etchant concentration E_a = activation energy

 E_R increases with E_a (Kcal/mol) N_x T (as a function of E_a)Si2.48SiO₂3.76

Temperature control of the wafer

Clamp or Electrostatic Chuck





V. M. Donnelly, A. Kornblit J. Vac. Sci. Technol. A, Vol. 31(5), 2013 FIG. 31. Various profiles obtained during plasma etching: (a) bowing due to faceting of the mask; (b) microtrenching due to enhanced ion flux along the sidewall; (c) Undercutting due to an isotropic component in the etch process; (d) tapered profile due to deposition on the sidewall; (e) notching at the interface due to inadequate sidewall passivation or charging effects; (f) Re-entrant profile (overcutting) due to inadequate sidewall passivation and/ or ion scattering.
Notch Effect

Notching effect due to charging oxide by ions

Can be reduced by using low frequency (LF) 380kHz bias generator in pulsed mode



RF bias RF bias on off



[J. Vac. Sci. Technol. B 19.5., Sep/Oct 2001]

STS ASE has LF pulsed generator!!

killer particles in microelectronics



avoid dust in plasma processing

DRY ETCHING IN FLUORINATED FEEDS

Production of volatile fluorides:

Si, SiO₂, Si₃N₄, W, Mo, Ti, TiN,

feeds utilized:

$$F_{2}$$
, CF_{4} , CF_{4}/O_{2} , CF_{4}/H_{2} , SF_{6} , SF_{6}/O_{2} , NF_{3} , XeF_{2}

- **CF**₄ is the most popular fluorine atom source
- similar approach with other fluorocarbons

F₂ is difficult to handle

CF₄ fragmentation :

$$CF_4 + e^- \implies CF_3 + F + e^-$$
$$CF_3 + e^- \implies CF_2 + F + e^-$$
$$CF_2 + e^- \implies CF_2 + F + e^-$$

F (etchant)

CF₃, CF₂, CF = CFx (radicals, insaturates)

CFx radicals can deposit fluoropolymer "teflon-like" coatings

The choice of the feed

- Si materials (Si, SiO₂, Si₃N₄) etch in Fluorine Chemistries (SiF₂ and SiF₄ volatile species)
- Fluorine-to-Carbon Ratio Model
 - Silicon etch rate





the chemistry of fluorocarbon plasmas can be changed with oxidizing and reducing additives

 $CF_x + O(O_2) \rightarrow CO, CO_2, COF_2 + x F$



PE-CVD OF FLUOROPOLYMERS ETCHING OF Si and SiO₂





fluoropolymer "teflon-like" coatings passivate sidewalls and improve etching anisotropy

when the radical density is high the deposition rate becomes too high and etching stops





Additive	Purpose ,	Example (Additive-Etchant Gas : Material)
Oxide Etchant	Etch through material oxide to initiate etching.	$C_2F_6 - Cl_2 : SiO_2;$ BCl_3 - Cl_2 : Al_2O_3; CCl_4 - Cl_2 : Al_2O_3
Oxidant	Increase etchant concentration or suppress polymer.	$O_2 - CF_4 : Si;$ $N_2O - CHF_3 : SiO_2;$ $O_2 - CCl_4 : GaAs, InP$
"Inert" Gas, N ₂	Stabilize plasma, dilute etchant, improve heat transfer.	Ar—O ₂ : organic material; He—CF ₃ Br : Ti
Inhibitor-Former	Induce anisotropy, improve selectivity.	$C_2F_6 - Cl_2 : Si;$ BCl ₃ - Cl ₂ : GaAs, Al H ₂ - CF ₄ : SiO ₂
Radical-Scavenger	Increase Film-Former, improve selectivity.	$H_2 - CF_4$ $CHF_3 - C_2F_6 : SiO_2;$ $H_2 - CF_4 : SiO_2$
Water/Oxygen- Scavenger	Prevent Inhibition improve selectivity.	$BCl_3 - Cl_2 : Al;$ $H_2 - CF_4 : SiO_2$
Volatilizer	Form a more volatile product,	$O_2 - Cl_2 : Cr, MoSi_2$

Table 8 Gas additives for plasma etching.

 $c-C_4F_8$ (octa fluorocyclobutane, F/C 2), $c-C_5F_8$ (octafluoro cyclopentene, F/C 1.6), and C_4F_6 (hexa fluoro-1,3-butadiene, F/C 1.5) were chosen in newer generation etchers. Although changing to these gases was driven primarily by performances, there were environmental considerations as well. $c-C_5F_8$, for instance, has short atmospheric lifetime (0.3 vs 3200 years for C_4F_8 and 270 for CHF₃) and reduced Global Warming Potential (GWP)

Comparisons were made of etching of high aspect-ratio contacts with $c-C_4F_8$ to $c-C_5F_8$ and C_4F_6 in a modified **GEC Reference Cell (a parallel plate reference reactor).** The performance of these gases may be different, though, depending on the etcher used.

Common additives include O_2 , Ar, CO_2 , and CO. The latter is used to control selectivity, since it minimizes the amount of F-rich species.

Special care is needed with CO since it reacts spontaneously with Nickel. All gas delivery hardware, thus, must avoid exposed Ni surfaces (e.g., Ni gaskets). 316 SS is acceptable gasket and tubing material for CO.

feeds with reduced Global Warming Potential (GWP)



FLUORINE PLASMAS DRY ETCHING OF Si (c-Si, 100, 111, polySi, nc-Si, p-Si, n-Si)

- ETCHANT SPECIES: F
- REACTION PRODUCTS: SiF₄ and SiF₂
- F atoms do not need ion bombardment to react with Si
- ion bombardment increases the etching rate and anysotropy
- ion energy threshold at about 10-15 eV
- high Si / SiO₂ selectivity (up to 40)

F is a strong etchant for silicon the reaction is rapid and spontaneous



Si etching in F-containing plasma is isotropic

anisotropy can be achieved:

at low P, with high substrate bias to enhance the ion bombardment (poor Si/SiO₂ selectivity)

at higher P (and, in general) increasing the concentration of film precursors (CF_x) by adding reducing agent (sidewall inhibitor)

GENERAL Si ETCHING MECHANISM

1) formation of active species

2) adsorption of active species

formation of a fluorinated layer 3-5 monolayers thick

3) formation of volatile products

SiF₃ emits at 500 nm

4) desorption of products

e.g.
$$CF_4 \rightarrow CF_x + 4-x F$$





MANY FEEDS CAN BE UTILIZED:

), CF_4 , CF_4 / O_2 , SF_6 / O_2 , NF_3 , etc.

F₂ is too reactive (F-F bond is weak), hazardous, very difficult to handle

CF₄ and SF₆ are easy to handle and generate high [F]

$$CF_4 \longrightarrow CF_3 + F \longrightarrow CF_2 + F \longrightarrow CF + F$$

CF_x radical deposit fluoropolymer "teflon-like" coatings

$CF_x + O(O_2) \rightarrow CO, CO_2, COF_2 + x F$



SI ETCHING IN CF_4/O_2 **RF GLOW DISCHARGES**

O₂ ASSISTS THE FORMATION OF CO, CO₂, COF₂ SPECIES

without O₂ addition:

 $E_{Si} = K_E[F]$

WITH OXYGEN ADDITION



oxygen competes with F in the chemisorption on the Si surface and in the passivation of Si to SiO₂ and reduces the etch rate





[F] and [O] both decrease when the area of exposed Si increases



LOADING

depletion of the etchant in the gas phase due to reaction with the substrate. Reduces the etch rate when the substrate surface exposed to the plasma increases.



R. D'AGOSTINO, D. L. FLAMM, J. APPL. PHYS., (1981), 52, 162

 SF_6 , SF_6 / O_2

SF_6 generates high [F] \rightarrow high E_R

loading and carbon contaminations are reduced

low anisotropy, high selectivity Si/SiO₂

to avoid S contaminations (whitish powder) O_2 is added:

 $S_x + 20 \rightarrow SO_2$ (volatile) $SF_6 + 0 \rightarrow SO_2 + F$

CHLORINE CONTAINING PLASMAS SILICON ETCHING

$Si + 4 Cl \implies SiCl_4$

- Cl₂ and other feeds are used
- spontaneous (no plasma) etching only for n-doped Si
- Cl adsorbed on Si does not allow the reaction of other species
- the reaction needs ion bombardment
- the anisotropy is high for Si and p-Si
- for highly n-doped Si inhibitor chemistry (side wall passivation) is needed to obtain anisotropy



The etch rate of n-doped Si with Cl is 15-25 times higher than that of undoped or P-doped (n-doped) Si

FIGURE 29. Etching of doped and undoped polysilicon using a Cl_2/C_2F_6 feed in a parallel plate reactor at 0.35 Torr, 200 sccm feed, 0.32 W/cm² and a 25°C electrode temperature. Cl atoms in chlorine-rich plasmas chemically etch *n*-type *P*-doped polysilicon, while the etch rate of undoped silicon is low. Species from C_2F_6 form a sidewall inhibitor layer which provides anisotropy. Beyond about 20% Cl₂ etching becomes isotropic because there is not enough inhibitor to prevent Cl-atoms from attacking doped polysilicon sidewalls. Species from C_2F_6 also remove native etch native oxide from the Si surface so etching can start (after [157]).

The chemical etching of silicon in halogen-based discharges is affected by the type and concentration of electrically active dopants. In F atom systems, p-type doping (boron) suppresses silicon etch rates slightly (by as much as a factor of two) [76, 77, 78, 79, 80], while high concentrations of *n*-type dopants (As or $P \ge 10^{19} \text{ cm}^{-3}$) enhance etching [76, 77, 78, 79, 81] by a factor of 1.5-2. By contrast heavily n-doped (100) and (111) silicon [82, 83, 84] and polysilicon [67, 85, 86, 87, 88, 89] (~ 10²⁰ cm⁻³) in Cl atom plasmas (Cl₂, Cl₂/Ar, CCl₄/Ar, CF₃Cl, SiCl₄/O₂, CF₃Br/Cl₂, C₂F₆/Cl₂) etch as much as 15-25 times faster than undoped substrates. This enhancement is related to the concentration of active n-type carriers (e.g., the Fermi level), rather than the chemical identity of the dopant [67, 79, 90, 91, 92]. Unannealed or electrically inactive dopant implants have a minimal influence on etching [67, 90].

The detailed mechanisms through which chlorine-silicon etch rates depend on doping levels are still being studied. However, it is generally agreed that *n*-type doping raises the Fermi level and thereby reduces the energy barrier for charge transfer to chemisorbed chlorine [67, 93, 156]. As depicted in Fig. 28, chlorine and/or bromine atoms are covalently bound to specific sites on an undoped silicon surface. Steric hindrance impedes impinging etchant from penetrating the surface to reach subsurface Si-Si bonds. The formation of a more ionic silicon-halogen surface bond, due to the *n*-type doping and enhanced electron transfer, opens additional chemisorption sites and facilitates etchant penetration into the substrate lattice.

Table 9	Feed gases and r	mechanisms for	plasma etching	various materials
with chlo	rine atoms.		acces (2)	

Source		Materials		Selective
Gas	Additive	Etched	Mechanism	Over
C1,	None	heavily n-doped Si	Chemical	SiO ₂
	C ₂ F ₆		Ion-inhibitor	
	SiCl ₄		Ion-inhibitor	
Cl,	None	Si	Ion-energetic	SiO.
CCI.	0,	3789	B-me	5102
SiCl ₄	0 ₂			
	SiCL			
	CCL			SiO. Some
Cl,	CHCI,	Al	Ion-inhibitor	resists.
	BCl ₃			Si ₃ N ₄
CI ₂	O ₂	MoSi ₂	Ion-energetic	SiO ₂
C1 ₂	None		Chemical-	SiO ₂ ,
1922		III-V	Crystallographic	Resists
	BC13	Semiconductors	Ion-inhibitor	
	CC14			
CCI₄	0 ₂			
SiCl ₄	O ₂			
Cl ₂	O2, H2O	III-V Alloys	Chemical-	AlGa, As.,
100		without Al	Crystallographic	Alln, Py, SiO ₂ , Si ₃ N ₄ ,
1022	0.2565			Resists
CF_2Cl_2	None	- 8		Ion-inhibitor

Bulk micromachining of Silicon

Silicon bulk micromachining requires to etch "holes" deeper than 10 μ m. It is defined as deep RIE or DRIE. Modified high plasma-density etchers are used, with additional features to facilitate high etch rates with profile control. **SF₆ is used** to achieve high etch rates, sometimes **with O₂** to reduce sulfur build-up. To obtain anisotropy, the sidewalls of the features to be etched must be passivated.

One approach is to cool the substrate to < 220 K and slow the rate of isotropic etching by F-atoms. Ion-assisted etching have little or no T dependence. The low T also leads to a buildup of SiOxFy byproducts on the sidewalls, that suppress isotropic etching and produces smoother sidewalls than the **Bosch process**, but time is needed for wafer cooling and warming before & after etch. Once the wafer is warmed, the protection is volatilized, and if additional etch time is needed fter post-etch inspection, under-cutting occurs due to the lack of a protection layer on the sidewall.



Fig. 41. Surface micromachining. The height of these features is $12 \mu m$, and the minimum dimension is $0.25 \mu m$.

The **Bosch Process** alternates **etching with** SF_6/O_2 and PE-CVD with c-C₄F₈ /Ar. The process requires fast mass-flow controllers to switch between etch and deposition, every few seconds. ICP etchers are used, and pulsed bias power at few watts only during the etch step. Source power during etching depends on the total gas flow. During PE-CVD a film is formed on horizontal surfaces and on sidewalls. The etch then removes the film from horizontal surfaces and etch Si, while the film on the sidewalls, even though eroded, protects against lateral etch. The resulting sidewalls show striations, and may be an issue when smooth sidewalls are needed. It is good to use etch mask and etch stop materials (if needed) resistant to F atoms. SiO₂, Al₂O₃, and PR masks etch very slowly with 250:1, >10,000:1, and 50:1 selectivity vs Si, respectively.

 SiO_2 and Al_2O_3 can be used as etch stop material. Care must be used in choosing such materials, in a way that they do not sputter nonvolatile products that would form "grass" in etched areas due to micromasking.

Etch depths are often hundreds of μ m, sometimes the full thickness of the wafer (700-750 μ m for 200 mm dia). High etching rate can be increased by increasing gas flow and source power. However, selectivity is reduced, since the etching rate of Si increases at a slower rate than the erosion of the mask, due to increased ion flux.



FIG. 42. Scalloping associated with a switched (Bosch) process. The scallops are the result of alternate etch and deposition steps.

STS ASE DRIE a 6" ICP Bosch process dedicated to Si etching

SF6/O2 and C4F8/Ar alternated feeds

High etch-rate recipe:

	Switching time	Pressure	RF coil power	RF bias power	Gas flow [sccm]
Etch	8.5 sec	40mTorr	2200W	40W	$450 \ \mathrm{SF_6}$
Passivation	3 sec	14mTorr	1500W	20W	$200~\mathrm{C_4F_8}$

high density

plasma reactor

Etch rate ≈ 8µm/min for 500 µm feature size with ~ 20% exposed area

High selectivity to PR ≈ 75-100





Bosch Process

Switching SF₆ and C₄F₈





The sidewall film thickness depends to the deposition or passivation time.

SUMMARY 1

In the 70s plasma etching became essential for pattern transfer in silicon ICs. As circuitry become more complex, with smaller and smaller features, the importance of plasma etching still increases.

Plasma etching began roughly 60 years ago when the undercutting of masks in wet etching was no longer tolerable. Si etching began in F-plasmas such as CF_4/O_2 , but it was quickly realized that the undercut by F atoms was not desirable and Cl-plasmas gave much better profiles. Parallel plate CCP reactors were used first for Si etching, then they were replaced by higher density ICP or MW plasmas.

Further improvements were realized by adding HBr to Cl₂. The etching of poly-Si and c-Si occurs by a mechanism where positive ions are accelerated by the voltage drop across the sheath, controlled by a separate bias applied to the substrate. This energetic ion bombardment disrupts the halogenated chemisorbed layer and gives volatile products.

Anisotropic Al etching of interconnects, developed with Cl-based CCP plasmas, later also migrated to higher density ICPs, with a quite different mechanism. Cl and Cl_2 react readily with Al without ion bombardment, which leads to severe mask undercut. To prevent this, BCl_3 or CClx photoresist erosion species are introduced, and bare Al is coated with a passivating layer that prevents chemical etching by Cl and Cl_2 . Positive ions keep horizontal surfaces quite clean, allowing chemical etch, with enhancement by ion bombardment. On vertical surfaces, the passivation layer prevents etching and leads to anisotropic profiles.

SUMMARY-2

SiO2 etch for patterned insulating layers between interconnecting Al wires and Si transistors began at the same time. **CFx- plasmas** emerged and remained the only way to achieve anisotropic SiO2 etching selective vs Si. SiO2 etching evolved from CCP to ICP and back to CCP etchers. The reemergence of CCP for SiO₂ etch was accompanied by using RF power at 2 (or 3) frequencies. The mechanism of SiO2 etching was well studied, due to its importance and complexity. **SiO₂ etching is due to a thin CFx film that also inhibits unwanted etching of Si**. Ion bombardment of the CFx layer generates SiF4, CO, CO2, and perhaps other products that must then diffuse through the layer.

Insulating materials with dielectric constants lower than SiO₂ (low-k materials) have emerged. These films usually contain Si, C, and O and often have voids to further reduce the dielectric constant. CFx-plasmas etch these materials with a mechanism similar to SiO₂, in the same equipment used to etch SiO₂.

Following the development for **Si, Al, and SiO2 patterning**, plasma was soon used **for etching other materials**. For the first 25 years or so, plasma etching was used strictly for transferring patterns from PRs to these materials, some of which (e.g., SiO2 and a-Si) were used as hard masks for underlying layers. In the last 25 years, however, many applications emerged where plasma etching is taking on more of the task traditionally carried out by photolithography. These involve a starting structure with a relatively wide linewidth and then creating 1, 2, or even 3 narrower lines by trimming processes or by depositing thin layers on the sides of lines to be then removed.

The number of such processes will certainly increase in the future.

SUMMARY-3

Future needs will go for tighter control of process variability, higher selectivity and less damage. This may require: pulsed plasmas, lower ion energies, tighter control of ion energy distributions, reduced photon fluxes.

Evolution to **Atomic Layer** or neutral beam Etching etching could become if sensitive necessary devices longer can no monolayer-scale tolerate produced by damage immersing substrates in the plasma.

Overview of atomic layer etching in the semiconductor industry

Keren J. Kanarik, Thorsten Lill, Eric A. Hudson, Saravanapriyan Sriraman, Samantha Tan, Jeffrey Marks, Vahid Vahedi, and Richard A. Gottscho

Citation: Journal of Vacuum Science & Technology A 33, 020802 (2015); doi: 10.1116/1.4913379



FIG. 1. (Color) Schematic of ALE (a) generic concept, (b) for the silicon case study, and (c) in comparison to ALD. ALE is similar to ALD except that removal takes place instead of adsorption in reaction B.

SUMMARY-4

Future devices will certainly have smaller critical dimensions, will incorporate new materials and structures, and will be fabricated on larger wafers. Although self-assembly is considered for some structures and materials, dry etching will still be used for most of the pattern transfer of the ever-shrinking lithographic features. In some cases, new materials will be incorporated in cavities of traditional SC materials, and in other cases, these materials will require dry etching, and new etching processes will have to be developed.

The choice of structures and materials will be influenced greatly by the capabilities of etching processes and equipment on hand. Control of selectivity (to the substrate and to the mask), profile, lattice damage, plasma damage (which may be enhanced by photon flux), particle formation, process reproducibility, and equipment reliability will dominate future etching technologies and equipment.

Plasma etching technology has evolved from a manually loaded quartz tube with a coil wound around it to sophisticated automatic multimillion dollar machines, with advanced equipment and process control. This evolution continues.

SiOx *quartz-like* plasma-deposited coatings

- dielectric layers in microelectronics
- gas/vapor barrier coatings for food and pharmaceutical packaging
- anti corrosion protective layers for car lights and other substrates

LOW GAS TRANSMISSION RATE (food, pharmaceutical packaging) **MW compatible** HARDNESS TRANSPARENCY **INERTNESS CORROSION PROTECTION SEAL COATING** (car lights) DIELECTRIC

PE-CVD from ORGANOSILICON / O₂ feeds Si(C,H)Ox ----- SiOx

Key Parameters
monomer/O ₂ ratio
input power (fragmentation)

	MONOM	ERS	
CH₃ CH₃ CH₃-Si-O-Si-CH₃ CH₃ CH₃	OCH ₂ CH3 I CH3CH ₂ O-Si-OCH ₂ CH3 I CH3CH ₂ O	CH3 CH3 CH3-Si-N-Si-CH3 CH3 H CH3	CH3 I CH3-Si-CH3 I CH3
HMDSO	TEOS	HMDSN	TMS

HMDSO/O2 RF GLOW DISCHARGES

DENSITY (A.U.)		Si		-	•	ОҢ, С	Ю Н
0	5 1	0 15	20	5	10	15	20
	O_2/H	MDSO		$O_{2^{\prime}}$	/HMDi	50	

Table II	. Spectral	Features
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Species	Feature	Wavelength (Å)
Si	$3p^{23}P-4s^{3}P^{0}$	2516.1
0	3s ⁵ S ⁰ -3p ⁵ P	7771.9
Н	$2p^2P^0-3d^2D$	6562.8
С	$2p^{21}S - 3s^{1}P^{0}$	2478.5
SiO	$A^{1}\Pi - X^{1}\Sigma^{+}$	2413.8
OH	$A^2\Sigma^+ - X^2\Pi$	3036.0
CH	$A^2\Delta - X^2\Pi$	4314.2
CO	$B^{1}\Sigma - A^{1}\Pi$	4835.3
Ar	4s'-4p'	7503.0
He	$2s^3S - 3p^3P^0$	3889.0

Relative concentration trends of (a) Si, SiO, C, O; (b) H, OH, CH and CO species in plasma phase as a function of feed composition.







Fig. 6. FT-IR spectra obtained from (a) HMDSO liquid monomer and from films deposited at: (b) 100% HMDSO; (c) O₂/HMDSO=2; (d) O₂/HMDSO=10; (e) O₂/HMDSO=20 feed composition.

72


PROCESS CONTROL

Silicone-like, SiO₂-like gas barrier coatings on PET



The gas transmission rate (O_2, H_2O) through the SiOx coating depends on its carbon content, which is a function of the density of CH (and C) radicals in the plasma phase.

AT HIGH O₂/MONOMER RATIO (very high barrier, highly inorganic coating) GTR DEPENDS ON Si-OH GROUPS IN THE COATINGS



100

0

200

Power (W)

300

the delivered power.

75





IR-AS PROCESS CONTROL

SiO₂-like gas barrier coatings on PET films for packaging

Fig. 4. A characteristic absorbance spectrum of an HMDSO/O₂ (3:17 gas flow rate ratio) plasma reported as $-\ln(T_p/T_g)$, where T_g and T_p are the gas phase (plasma off) and the plasma phase transmittance, respectively. The band marked with (*) has been attributed to the CH₃ bending in Si(CH₃)_x.





silanols (Si-OH) moieties open

OTR (Cm³/m² day atm)

multilayer stacks improve barrier performances



Graff el al., Journal of Applied Physics, Vol. 96, pp. 1840, 2004



organic layers decouple the defects of two inorganic layers and heals some defects of the next inorganic coating.

SiO_x FOR CORROSION PROTECTION ON METALS/ALLOYS

- Anti-tarnishing silver, copper and brass.
- Jewellery, Mint,
- anti-scratch for gold and polymers
- antiscratch for plastic windshields and windows (subway of Nagoya)
- Anti-stain for marble and granites
- barrier films for packaging
- superbarrier for flexible electronics

PE-CVD SiOx "protecting seal" coatings on Al-evaporated plastic car lights



rivestimento protettivo SiOx su metalli (Al)

dopo 48 h in camera a nebbia salina



non trattato



trattato





PROTECTION FROM CORROSION: AVOIDING TARNISHING ON SILVER

Silver (and other metal) surfaces darken easily with time for air exposure, due mainly to reactions with S-containing molecules that form sulphides/oxides layers. Technological, artistic and archaeological artefacts undergo a gradual darkenig known as *tarnishing*.



$2 \operatorname{Ag} + \operatorname{S}^{2-} \rightarrow \operatorname{Ag}_2 \operatorname{S} + 2 \operatorname{e}^{-}$	E ₀ =0,93 V (SCE)
$2 \operatorname{Cu} + \operatorname{S}^{2-} \operatorname{Cu}_2 \operatorname{S} + 2 \operatorname{e}^{-}$	E ₀ =1,17 V (SCE)
$Cu + S^{2-} \rightarrow CuS + 2e^{-}$	E ₀ =0,97 V (SCE)





PE-CVD SiOx



trattamento anti-tarnishing e anti ossidazione monete e medaglie argento, rame



H₂ plasma cleaning





bracciali in argento e rame



zona protetta via plasma dopo 10 cicli di *tarnish* test (*tarnish* accelerato in NaS 0.1 M)

zona non trattata dopo 10 cicli di *tarnish* test

http://www.ion-med.com/how.asp

AP plasmas for biomedicine

Two basic principles







Dimensions:	L = 155 mm, Ø = 20 mm
Weight:	170 g
HF-Voltage:	1.1 MHz; 2…6 kV _{pp}
Gas temp.:	30-50°C
Feed gas:	Argon
Gas flow:	3-5 slm

Atmopheric pressure plasma jet kINPen MED



Certified as **medical device class lla** (June 2013) according to European Council Directive 93/42/EEC

<u>Purpose:</u> Treatment of chronic wounds as well as pathogenbased diseases of skin, skin appandages, extremities and body

K.-D. Weltmann, E. Kindel, R. Brandenburg, C. Meyer, R. Bussiahn, C. Wilke, Th. von Woedtke. Contrib. Plasma Phys. 49 (2009) 631-640; S. Bekeschus, A. Schmidt, K.-D. Weltmann, Th. von Woedtke. Clin. Plasma Med. 4 (2016) 19–28; S. Reuter, Th. von Woedtke, K.-D. Weltmann. J. Phys. D: Appl. Phys. 51 (2018) 233001;

www.neoplas-tools.eu







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Sample

В





plasma sterilization in hospitals

(136) STERRAD Plasma Sterilization Technology -YouTube



Decontamination / Sterilization

decontaminazione gusci d'uovo



L. Ragni et al. / Journal of Food Engineering 100 (2010) 125–132 decontaminazione in-pack di mele



Safe-bag project

decontaminazione di foglie di valeriana



M. Baier et al., Innovative Food Science & Emerging Tech 22 (2014) 147–157

decontaminazione di fette di cetriolo, carota, pera



R.X. Wang et al./ Eur. Phys. J. D (2012) 66: 276