CORSO DI STUDIO *Physics (LM-17)*
ANNO ACCADEMICO *2024-2025*
DENOMINAZIONE DELL'INSEGNAMENTO *Laboratory of Digital Devices*

General information	
Year of the course	1st
Academic calendar (starting and ending date)	1st semester: September – December 2024
Credits (CFU/ETCS):	6
SSD	FIS/01
Language	English
Mode of attendance	Compulsory

Professor/ Lecturer	
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Department and address	Physics Department, via Amendola 173, Bari
Virtual room	
Office Hours (and modalities: e.g., by appointment, on line, etc.)	Wednesday, by appointment (also other days).

Work schedule			
Hours			
Total	Lectures	Hands-on (laboratory, workshops, working groups, seminars, field trips)	Out-of-class study hours/ Self-study hours
150	24	45	81
CFU/ETCS			
6	3	3	

Learning Objectives	
Course prerequisites	Basic Analog Electronics, transistor MOS-FET and BJT

Teaching strategie	Classroom lessons / tutorials, supported by video projector and with the help of networked PCs. CAD design in laboratories in groups of max. 2 students with the realization, simulation and testing of digital circuits
Expected learning outcomes in terms of	
Knowledge and understanding on:	• Understanding the scientific method, the nature, and the methods of research in Physics • Knowledge of advanced computer tools commonly used in basic and applied research • Fundamentals of digital electronics and logic design of combinatorial and sequential circuits
Applying knowledge and understanding on:	• Ability to identify the essential elements of a phenomenon • Ability to use analogy to apply known solutions to new problems (problem solving) • Ability to use analytical and numerical mathematical computation tools

	● Ability to use electronic and computer technologies and their application to experimental data acquisition ● professional electronic CAD for logic design and simulation of digital circuits . Design and test of logical circuits to solve real problems in physics , industrial , medical and environmental fields.
Soft skills	● **Making informed judgments and choices** ● Ability to work with increasing levels of autonomy, including taking responsibility in project planning and managing facilities. ● awareness of safety issues in laboratory activities ● Ability to analyze a problem and to propose the most appropriate electronic (circuit and technology) solution. ● **Communicating knowledge and understanding** ● Competence in communication in Italian and English in advanced fields of Physics ● Ability to work in a group and to develop strategies for problem solving by comparing with colleagues and teachers. ● **Capacities to continue learning** ● Acquisition of basic knowledge tools for continuous learning and knowledge updates ● Ability to consult bibliographic material, databases and material on internet.
Syllabus	

Content knowledge	**Number Systems and Conversion.** **Boolean Algebra.** **Appendix CMOS gates.** Analog and digital signals. Binary numbers. Number systems conversion. Binary variables and true or false logic. Logic functions symbols, truth tables and timing diagrams: gates AND, OR, NOT, XOR, NAND and NOR. Electrical circuits to implement logic functions: MOS and BJT transistor as switches. Totem-pole configuration. CMOS structure for NAND and NOT gates. CMOS and TTL logic families. Definition of logical levels and noise margins. Features of the logic gates: fan-out, propagation time, the rise and fall times. Examples of datasheets for integrated circuits SSI: 74LS00, 74HCT00, 74LS04,74HCT04. **Boolean algebra and Applications.** **Multi-level Gate circuits NAND and NOR .** **Application of Boolean Algebra Minterm and Maxterm.** **Karnaugh Maps.** Axiomatic definition Boolean algebra. fundamental theorems and proofs. Boolean functions. Analysis of Boolean functions and their representation as logic circuits. Complement of Boolean functions. The logic functions using NAND or NOR gates. Standard forms of Boolean functions. Transformation of a Boolean function in standard form. Examples of realization of Boolean functions by means of logic gates. Process of synthesis of Boolean functions. Minimization of Boolean functions; Method of Karnaugh maps; Maps with 3 and 4 variables. Minimum form of a Boolean function, as sum of products or product of sums expressions. Condition "don't care". Arithmetic functions: binary numbers addition and subtraction. Circuits half adder and full adder, carry-look-ahead. **Combinatorial Circuit design using gates.** **Multiplexers, Decoders, and Programmable Logic devices.** Introduction to combinational logic circuits. External control of logic function using gates. Open Collector gates and wired logic. Tri-state gates and bus transmission of data, examples of datasheets for integrated 74LS125 and 74LS241. Multi-levels logical circuits and propagation delay: static and dynamic hazard. Procedures for the design of logic circuits: multiplexer, demultiplexer / Date Selector, Decoder and programmable circuits, Decoder BCD to seven segments, Encoder with priority. Codes: BCD, Gray, Excess3. Programmable devices: ROM, PLD, PROM, PAL. Field Programmable Gate Array (FPGA): Structure and Hardware description logic language (Verilog). **Sequential circuits: Latches and Flip-Flops; Register and counters.** Sequential circuits definition. Analysis of asynchronous sequential circuits. Latch Set /Reset . Synchronous sequential circuits. S-R Flip Flop. JK Flip-Flop and JK Master-Slave. D type Flip-flop and T type. Edge-triggered flip-flop. Registers (examples: datasheet for 74LS373 and 74LS374). Shift-register. FIFO and RAM memories. Asynchronous Counters. **Analysis of Clocked Sequential circuits** Characteristics equations of flip-flops. Analysis of synchronous sequential circuits. Table of States and States Graph. Design of Binary Counters circuits with T and D Flip Flop. **Laboratory experiments** - Propagation delay measurement of NAND gates;

	Synthesis, simulation and implementation of combinational and sequential circuits. Design and simulation of digital circuits using PSPICE CAD: -A 2 Bit Comparator; -A Circuit for the data transmission on a 3-State bus; -A Display using a Decoder BCD-seven segments; -A Decoder project by programming a PLD GAL16V8 ,with the OrCAD PLD program including simulation in /out; -A Decimal 2 digit asynchronous Counter; -A 4 bit synchronous counter using D and T Flip Flop ; -FPGA Circuits Design and Simulation with VERILOG and ISE.
Texts and readings	-C. H. Roth , L. Kinney; Cengage Learning " Fundamentals of logic designs " ; -Millman-Grabel; Ed. Mc Graw Hill " Microelettronics "; -OrCAD Pspice , ORCADPLD tutorial , datasheet of electronic components (ex. http://www.alldatasheet.com/) .
Notes, additional materials	Slides from lessons
Repository	

Assessment	
Assessment methods	
Assessment criteria	● **Knowledge and understanding** of basic logical circuits and methodologies for the analysis and synthesis of combinatorial and sequential logic circuits and how to design and simulate combinatorial and sequential circuits using electronic CAD. ● **Applying knowledge and understanding** to identify and implement the logical circuit that solves problems of applicative nature, also through group discussions or discussions with the teacher . ● **Autonomy of judgment** Understanding of the simulation results to improve the designed circuits. ● **Communicating knowledge and understanding** writing laboratory experience reports. ● **Communication skills** Ability to present the results of an experiments effectively in written and oral form. ● **Capacities to continue learning** how to consult bibliographic material, databases and material on internet.
Final exam and grading criteria	Laboratory circuits design, simulation and test . Oral examination.
Further information	
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